



## TFT LCD Approval Specification

# Model No.: V260B3-LE1

Customer: \_\_\_\_\_

Approved by: \_\_\_\_\_

Note:

Approved By	TV Product Marketing & Management Div	
	Chao-Chun Chung	

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	TC Pan

Prepared By	LCD TV Marketing and Product Management Div.	
	Vincent Chou	Chi-Yao Lo



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**Approval**

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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver.2.0	Apr. 29,'10	All	All	Approval Specification was first issued.



## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V260B3-LE1 is a TFT Liquid Crystal Display module with LED Backlight unit and 1ch-LVDS interface. The display diagonal is 26". This module supports 1366 x 768 WXGA format and can display 16.7M colors (8-bit/color).

### 1.2 FEATURES

- Optimized Brightness 400nits
- Contrast Ratio (3000:1)
- Fast Response Time (Gray to Gray Average 8.5ms)
- Color Saturation NTSC 72%
- WXGA (1366 x 768 pixels) Resolution
- DE (Data Enable) Only Mode
- LVDS (Low Voltage Differential Signaling) Interface
- Viewing Angle: 176(H)/176(V) (CR>20) MVA Technology
- Color Reproduction (Nature Color)

### 1.3 APPLICATION

- TFT LCD TVs
- Optimized Brightness, Multi-Media Displays

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	575.769 (H) x 323.712 (V) (26" Diagonal)	mm	(1)
Bezel Opening Area	580.2 (H) x 328.2 (V)	mm	
Driver Element	a-si TFT Active Matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch(Sub Pixel)	0.1405 (H) x 0.4215 (V)	mm	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive Mode / Normally Black	-	-
Surface Treatment	Anti-Glare Coating (Haze 11%) Hard Coating (3H)	-	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

### 1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	612	613	614	mm	Module Size
	Vertical (V)	360	361	362	mm	
	Depth (D)	9.3	10.3	11.3	mm	To Rear
		16	17	18	mm	To CNV Cover
	Weight		2650		g	

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	50	°C	(1), (2)
Shock (Non-Operating)	S <sub>NOP</sub>	-	50	G	(3), (5)
			50		
Vibration (Non-Operating)	V <sub>NOP</sub>	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-Bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.

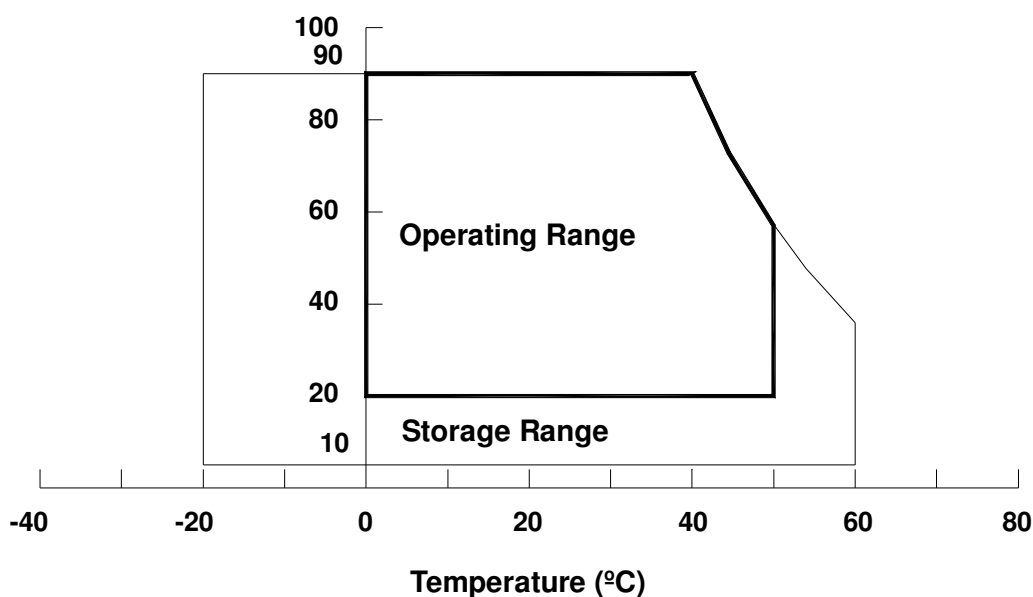
Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing of Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

**Relative Humidity (%RH)**



**2.2 ELECTRICAL ABSOLUTE RATINGS****2.2.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V <sub>CC</sub>	-0.3	13.5	V	(1)
Input Signal Voltage	V <sub>IN</sub>	-0.3	3.6	V	

**2.2.2 BACKLIGHT CONVERTER UNIT**

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V <sub>W</sub>	Ta = 25 °C	-	-	40.8	V <sub>RMS</sub>	
Converter Input Voltage	V <sub>BL</sub>	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

### 3. ELECTRICAL CHARACTERISTICS

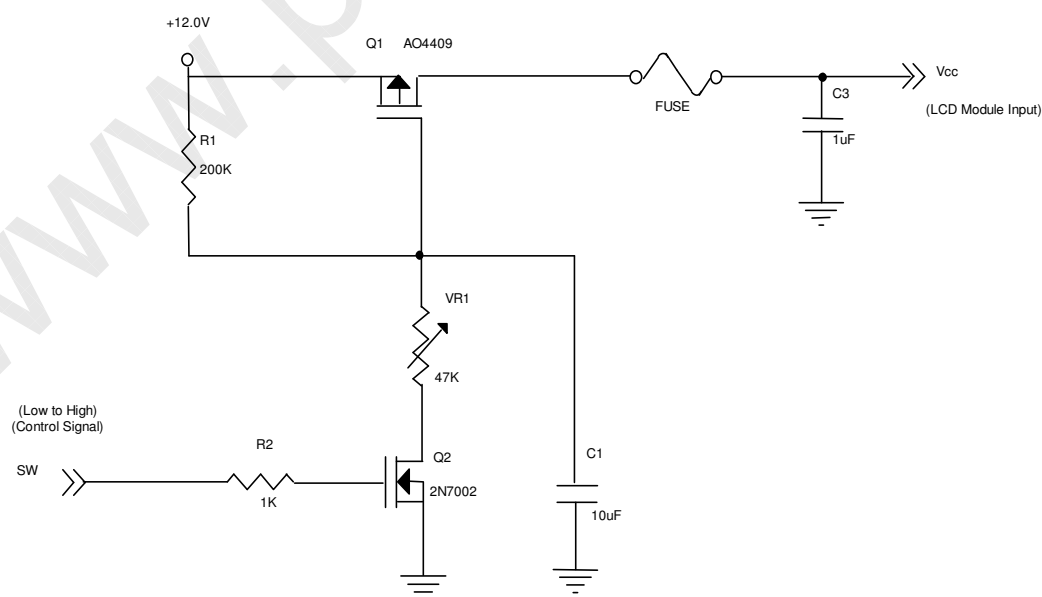
#### 3.1 TFT LCD MODULE

 $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ 

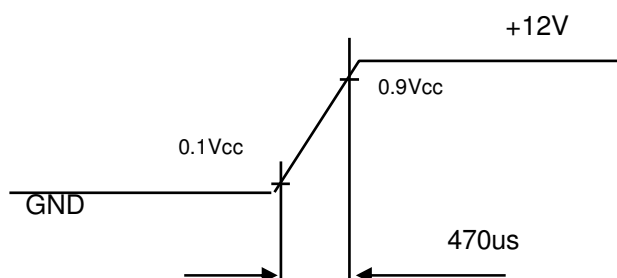
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		$V_{CC}$	10.8	12	13.2	V	(1)
Rush Current		$I_{RUSH}$	—	—	2.53	A	(2)
Power Supply Current	White Pattern	—	—	0.45	--	A	(3)
	Horizontal Stripe	—	—	0.56	0.65	A	
	Black Pattern	—	—	0.36	--	A	
LVDS interface	Differential Input High Threshold Voltage	$V_{LVTH}$	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	$V_{LVTL}$	—	—	-100	mV	
	Common Input Voltage	$V_{CM}$	1.0	1.2	1.4	V	
	Differential input voltage (Single-End)	$ V_{ID} $	200	—	600	mV	
	Terminating Resistor	$R_T$	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	$V_{IH}$	2.7	—	3.3	V	
	Input Low Threshold Voltage	$V_{IL}$	0	—	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Condition as below:





**Vcc rising time is 470us**

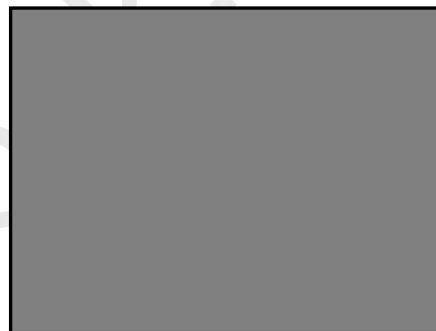
Note (3) The specified power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power-dissipation checking pattern is displayed as below.

a. White Pattern



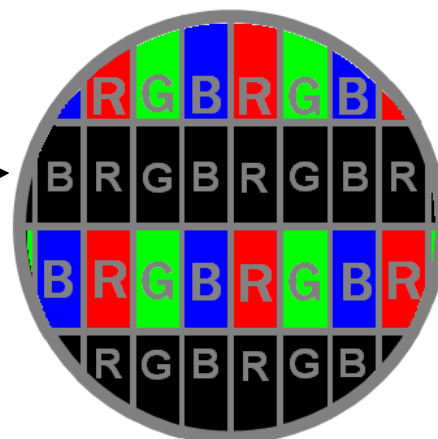
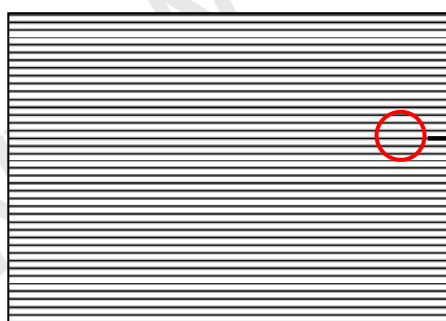
Active Area

b. Black Pattern

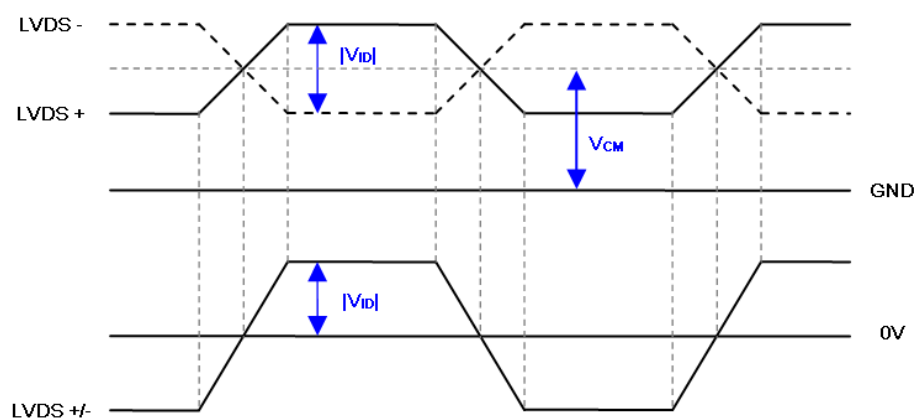


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



### 3.2 BACKLIGHT UNIT

#### 3.2.1 LED LIGHT BARCHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V <sub>W</sub>	-	-	40.8	V <sub>RMS</sub>	I <sub>L</sub> = 80mA
Forward Voltage	V <sub>f</sub>	-	3.1	3.4	V <sub>RMS</sub>	I <sub>L</sub> = 80mA
LED Current	I <sub>L</sub>	75.2	80	84.8	mA <sub>RMS</sub>	
LED lifetime	hr	30,000	-	-	hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, I<sub>L</sub> = 80mA

#### 3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL</sub>	-	29	33	W	
Converter Input Voltage	V <sub>BL</sub>	22.8	24	25.2	V <sub>DC</sub>	
Converter Input Current	I <sub>BL</sub>	-	1.2	1.4	A	
Dimming Frequency	F <sub>B</sub>	150	160	170	Hz	
Minimum Duty Ratio	D <sub>MIN</sub>	5	10	-	%	(1)

Note (1) 5% minimum duty ratio is only valid for electrical operation.

## 3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.0	3.15	3.3	V	Max. Duty Ratio
	MIN		—	—	0	—	V	Min. Duty Ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Error Signal		ERR	—	—	—	—	—	Abnormal: Open Collector Normal: GND (4)
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V <sub>BL</sub>
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	
PWM Delay Time		TPWM	—	100	—	—	ms	
BLON Delay Time	T <sub>on</sub>		—	300	—	—	ms	
	T <sub>on1</sub>		—	300	—	—	ms	
BLON Off Time		Toff	—	300	—	—	ms	

Note (1) The Dimming signal should be valid before backlight is turned on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight had been turned on period.

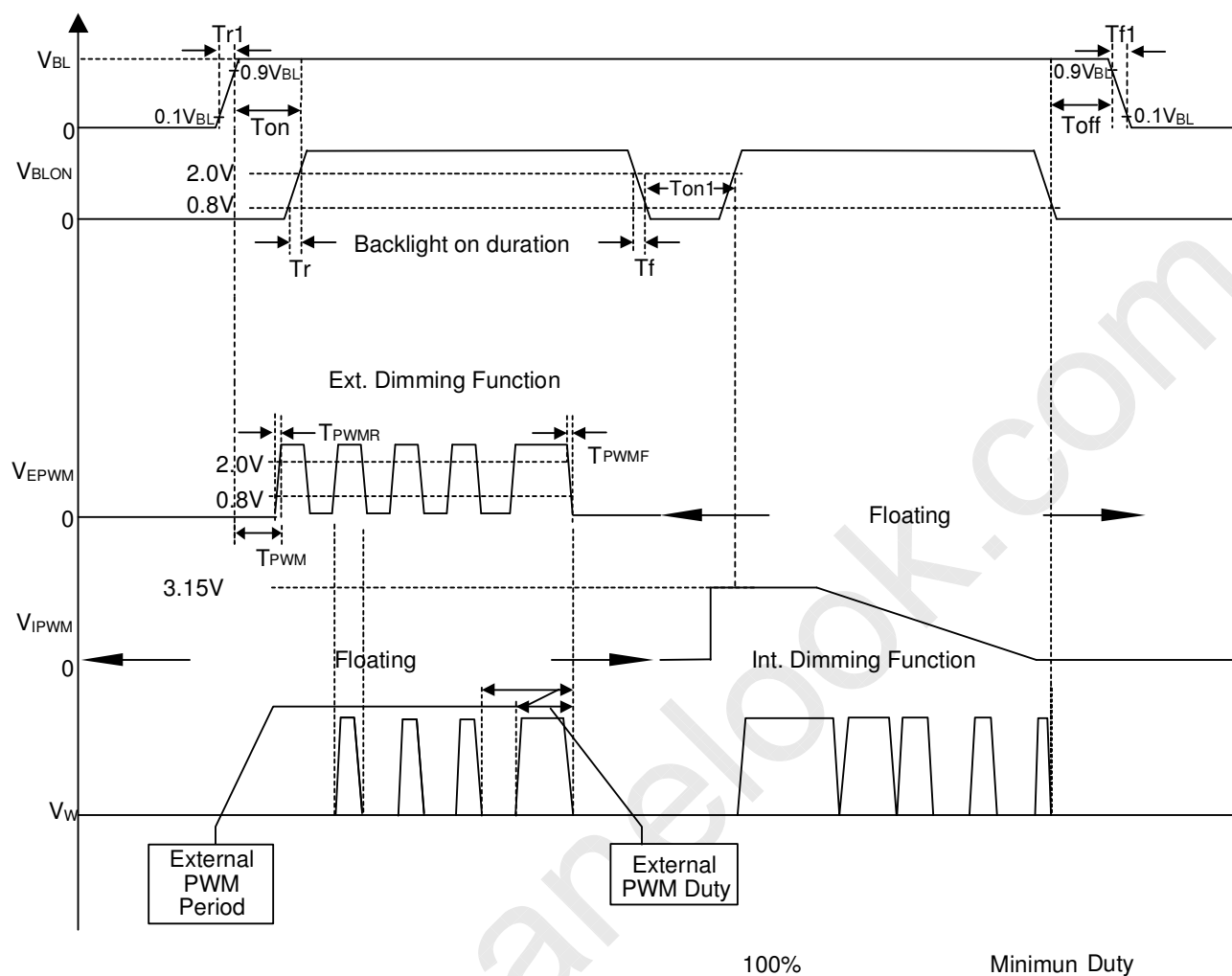
Note (2) The power sequence and control signal timing is shown in the following figure. For a certain reason, the converter is possible to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

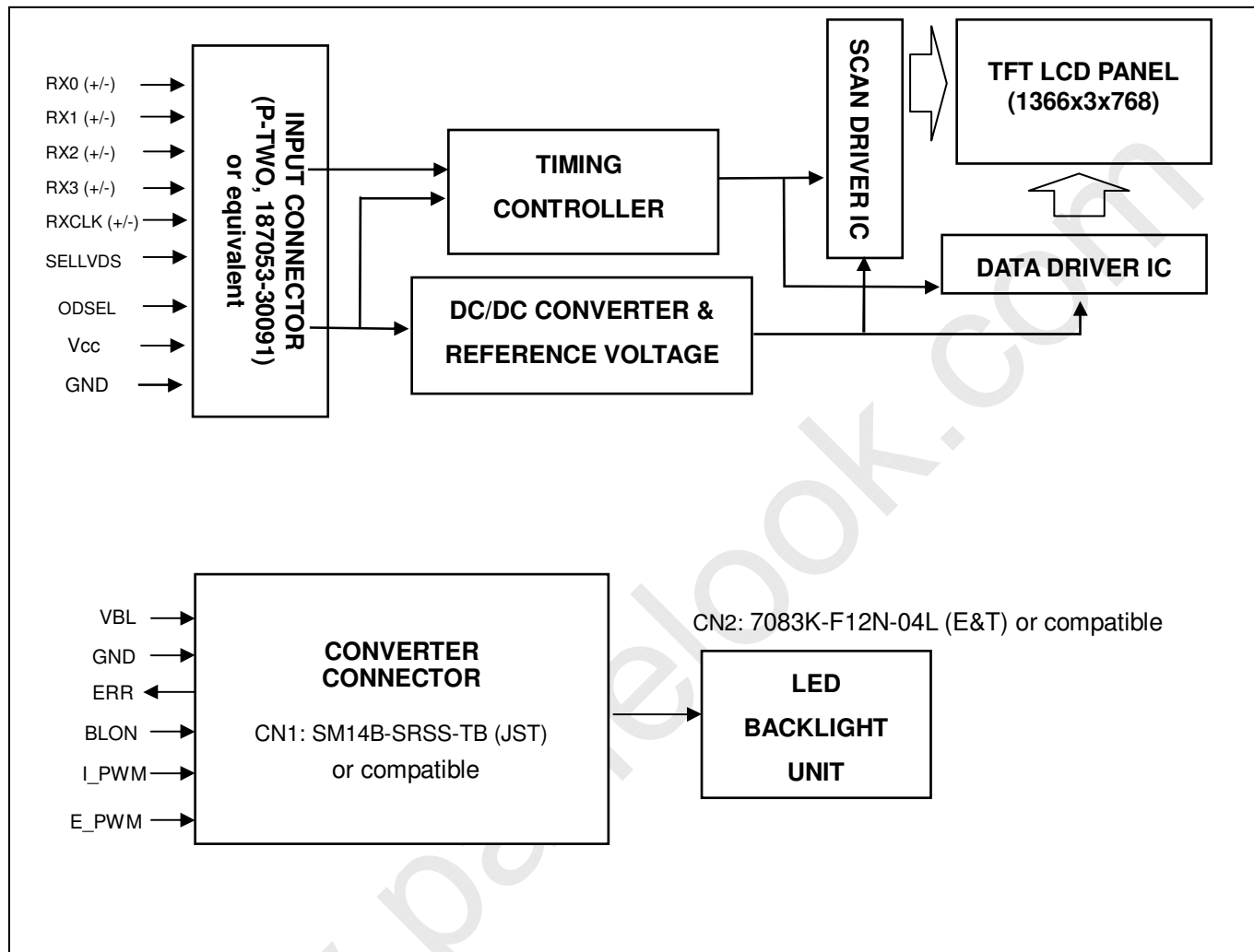
Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When the protective function of converter is triggered, ERR will output at open collector status.



## 4. BLOCK DIAGRAM OF INTERFACE

### 4.1 TFT LCD MODULE



## 5. INTERFACE PIN CONNECTION

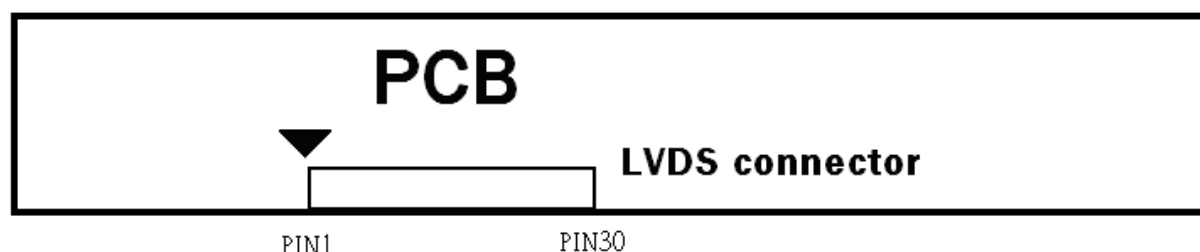
### 5.1 TFT LCD MODULE

#### CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VCC	Power supply: +12V	
2	VCC	Power supply: +12V	
3	VCC	Power supply: +12V	
4	VCC	Power supply: +12V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	NC	No connection	(4)
9	SELLVDS	Select LVDS data format	(2),(5)
10	ODSEL	Overdrive Lookup Table Selection	(3),(5)
11	GND	Ground	
12	RX0-	Negative transmission data of pixel 0	
13	RX0+	Positive transmission data of pixel 0	
14	GND	Ground	
15	RX1-	Negative transmission data of pixel 1	
16	RX1+	Positive transmission data of pixel 1	
17	GND	Ground	
18	RX2-	Negative transmission data of pixel 2	
19	RX2+	Positive transmission data of pixel 2	
20	GND	Ground	
21	RXCLK-	Negative of clock	
22	RXCLK+	Positive of clock	
23	GND	Ground	
24	RX3-	Negative transmission data of pixel 3	
25	RX3+	Positive transmission data of pixel 3	
26	GND	Ground	
27	NC	No connection	(4)
28	NC	No connection	(4)
29	NC	No connection	(4)
30	GND	Ground	

Note (1) Connector Part No.: P-TWO, 187053-30091 or compatible

The pin order of LVDS connector is defined as follows



Note (2) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

Please refer to 5.5 LVDS INTERFACE

Note (3) Overdrive lookup table selection. The Overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

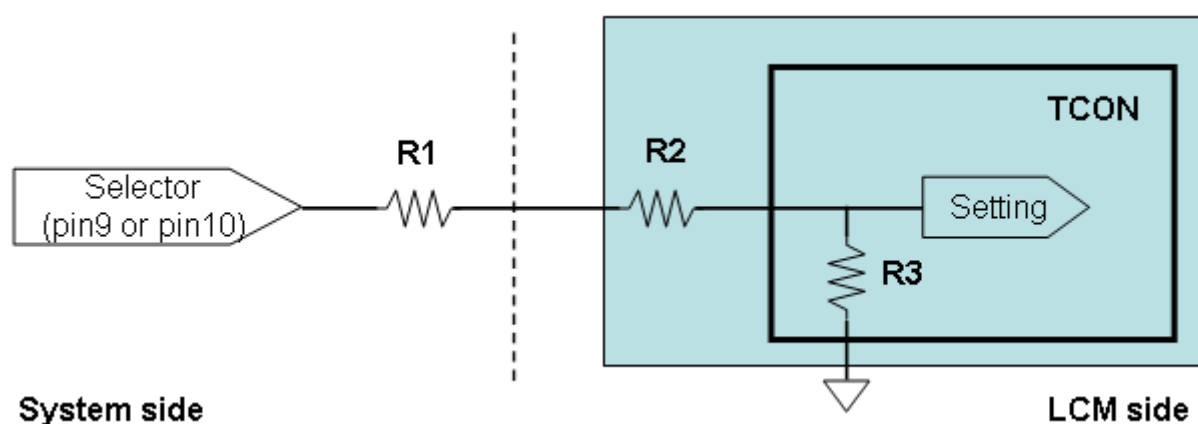
Low = Open or connect to GND, High = Connect to +3.3V

ODSEL	Note
L or Open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (4) Reserved for internal use. Let it open.

Note (5) LVDS signal pin connected to the LCM side followed the following diagram.

R1 in the system side should be less than 1K Ohm. ( $R1 < 1K\ \Omega$ )



## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table as below.

CN: 7083K-F12N-04L (E&T) or compatible

Pin №	Symbol	Feature
1	VLED+1	Positive of LED String
2	VLED+2	
3	NC	NC
4	NC	
5	VLED-	Negative of LED String
6	VLED-	
7	VLED-	
8	VLED-	
9	VLED-	
10	VLED-	
11	VLED-	
12	VLED-	

## 5.3 CONVERTER UNIT

CN1 (Header): SM14B-SRSS-TB (JST) or compatible

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	I_PWM	Internal PWM Control
14	E_PWM	External PWM Control

Note (1) PIN 13: Internal PWM Control (Use Pin 13): Pin 14 must open.

Note (2) PIN 14: External PWM Control (Use Pin 14): Pin 13 must open.

Note (3) Pin 13 (I\_PWM) and Pin 14 (E\_PWM) can't open in the same period.



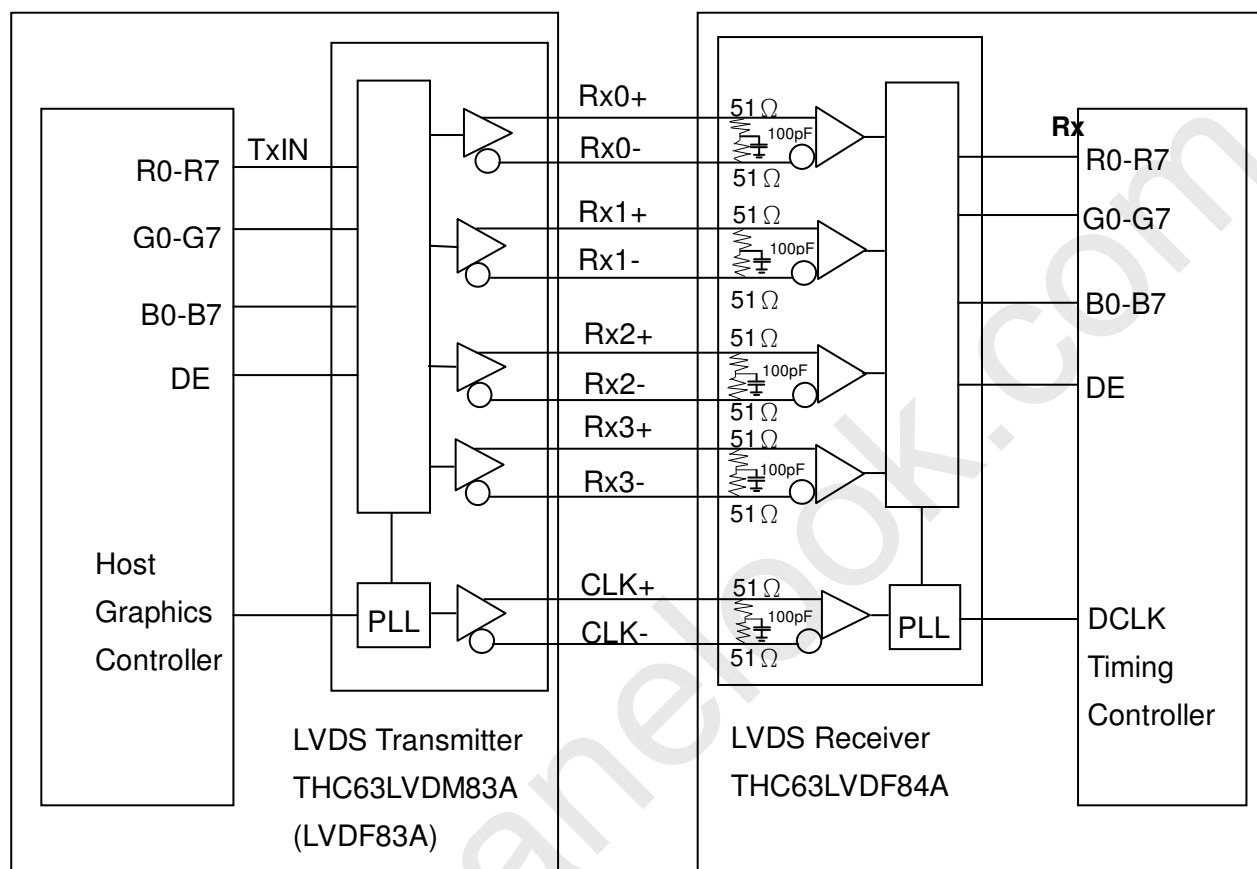


CN2 (Header): 7083K-F12N-04L (E&amp;T) or compatible

Pin №	Symbol	Feature
1	VLED+1	Positive of LED String
2	VLED+2	
3	NC	NC
4	NC	
5	VLED-	Negative of LED String
6	VLED-	
7	VLED-	
8	VLED-	
9	VLED-	
10	VLED-	
11	VLED-	
12	VLED-	

## 5.4 BLOCK DIAGRAM OF INTERFACE

CNF1



R0~R7 : Pixel R Data

G0~G7 : Pixel G Data

B0~B7 : Pixel B Data

DE : Data Enable Signal

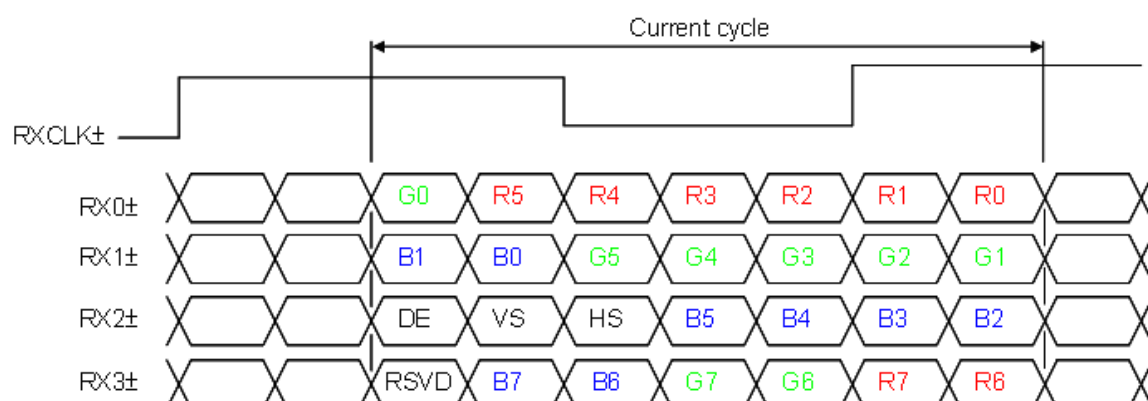
DCLK : Data clock signal

Note (1) The system must have the transmitter to drive the module.

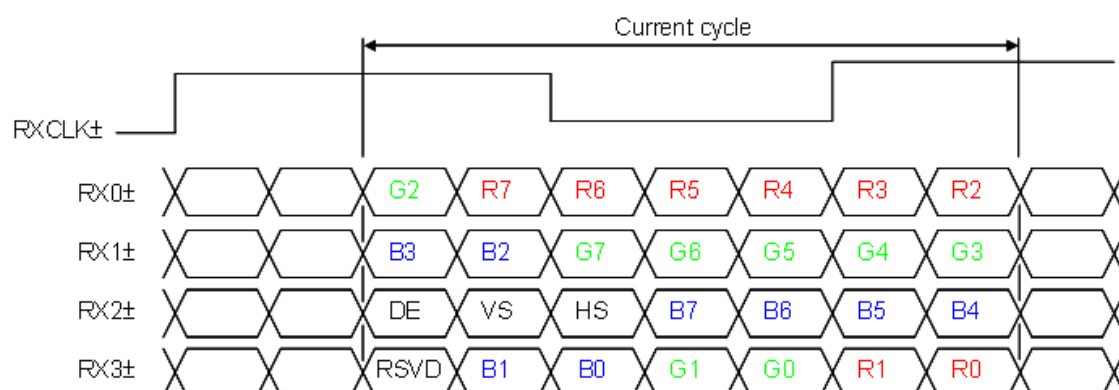
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

## 5.5 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=L or open)



JEDIA LVDS format : (SELLVDS pin=H)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes (1) RSVD (reserved) pins on the transmitter shall be "H" or ( "L" or OPEN)

## 5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The below table provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

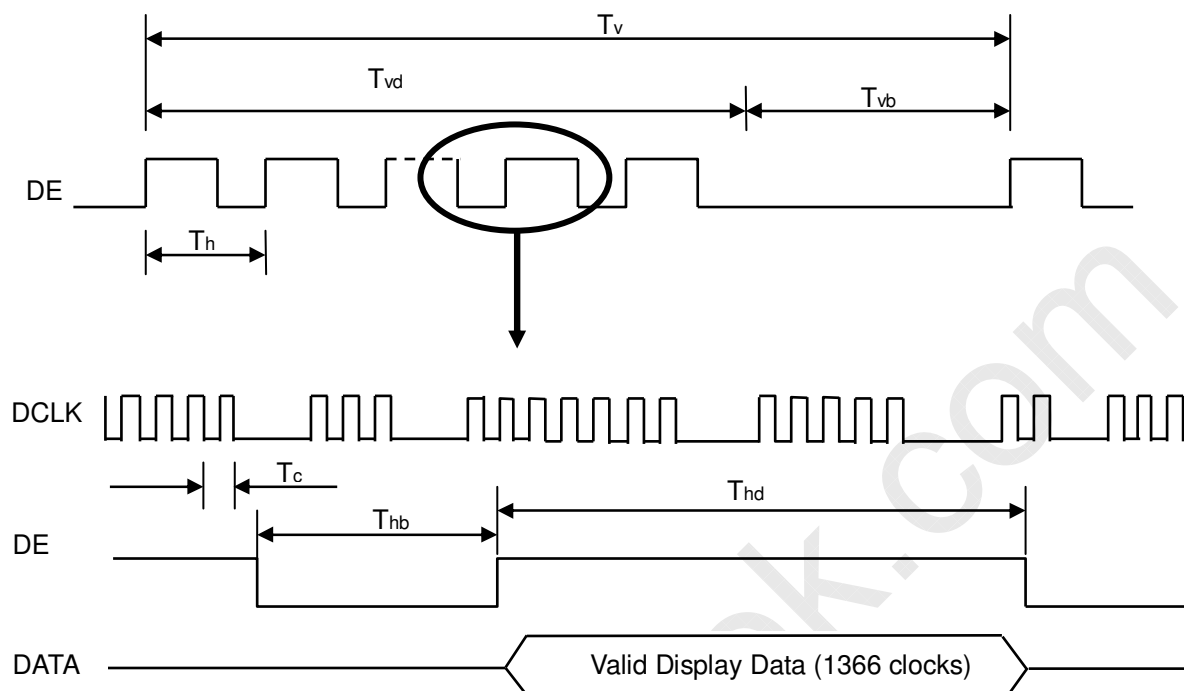
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}} (=1/TC)$	60	76	82	MHz	
	Input cycle to cycle jitter	$T_{\text{rcl}}$	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin\_mod}}$	$F_{\text{clkin}}-2\%$	—	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{\text{SSM}}$			200	KHz	
LVDS Receiver Data	Setup Time	$T_{\text{lvsu}}$	600	—	—	ps	(5)
	Hold Time	$T_{\text{lvhd}}$	600	—	—	ps	
Vertical Active Display Term	Frame Rate	$F_{\text{r5}}$	47	50	53	Hz	(6)
		$F_{\text{r6}}$	57	60	63	Hz	
	Total	$T_{\text{v}}$	778	806	888	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	$T_{\text{vd}}$	768	768	768	Th	—
	Blank	$T_{\text{vb}}$	10	38	120	Th	—
Horizontal Active Display Term	Total	$T_{\text{h}}$	1442	1560	1936	Tc	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	$T_{\text{hd}}$	1366	1366	1366	Tc	—
	Blank	$T_{\text{hb}}$	76	194	570	Tc	—

Note (1) Please make sure the range of pixel clock has followed the below equation :

$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

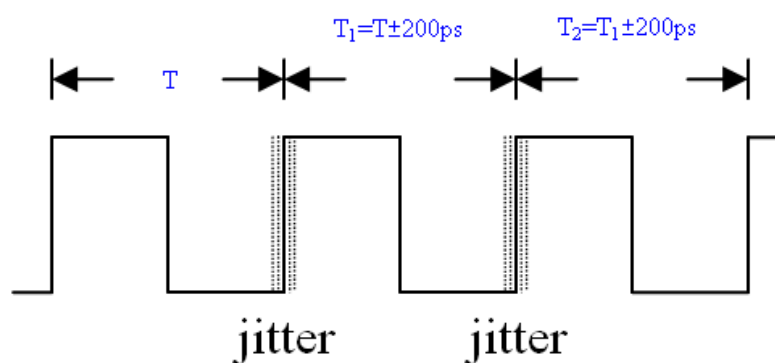
$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram as below :

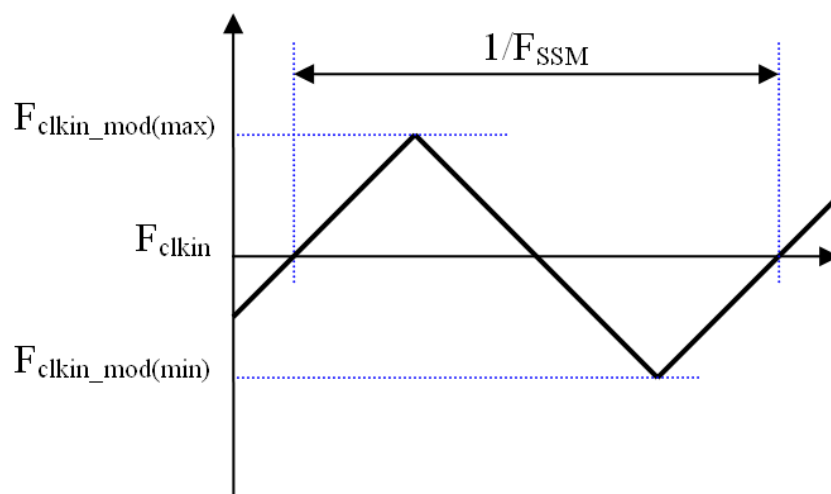
**INPUT SIGNAL TIMING DIAGRAM**

Note (3) The input of the clock cycle-to-cycle jitter is defined as below figure.

$$Trcl = |T_1 - T_2|$$

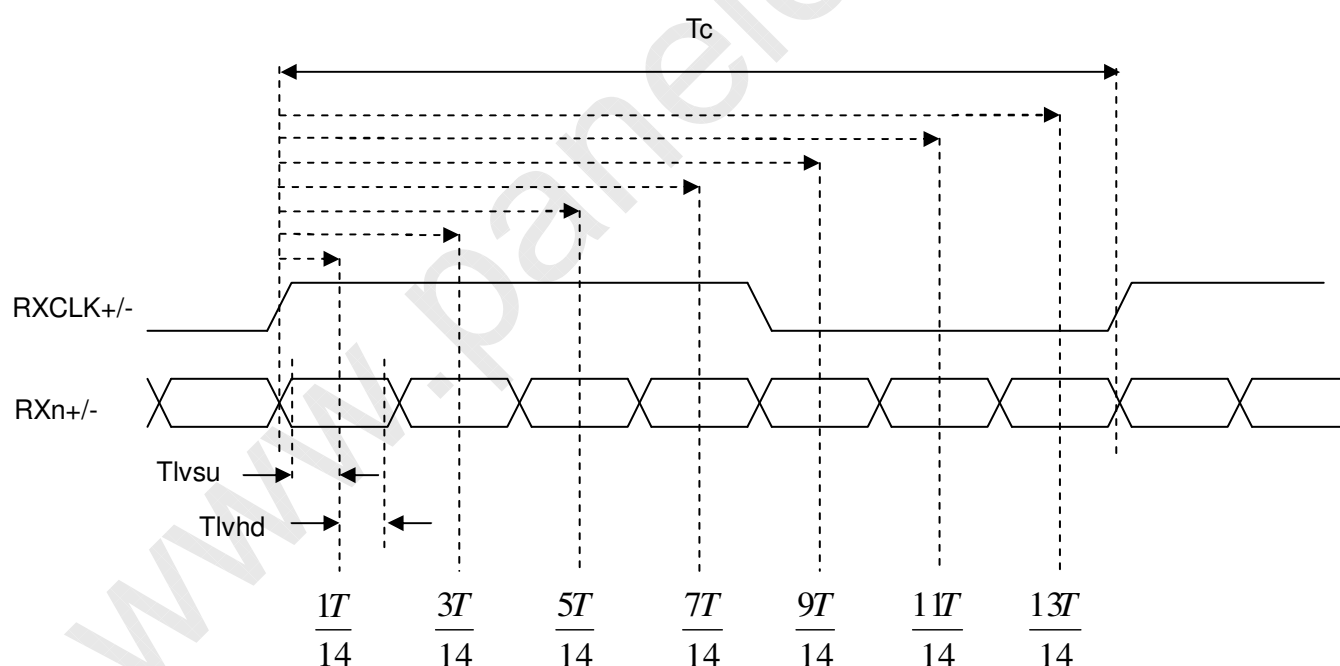


Note (4) The SSCG (Spread Spectrum Clock Generator) is defined as below figure.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figure.

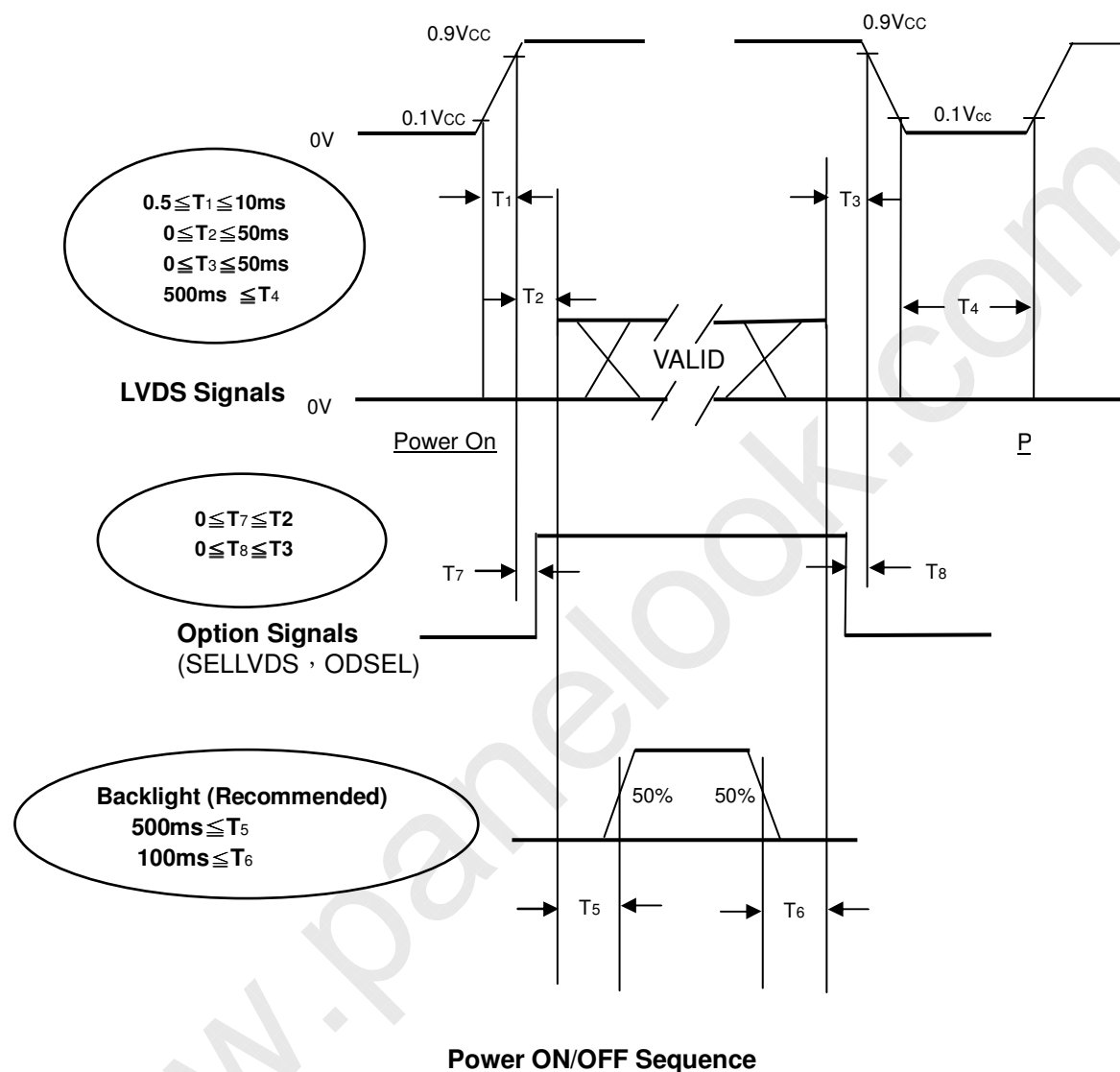
#### LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) (ODSEL) = H/L or open for 50/60 Hz frame rate. Please refer to 5.1 for detail information.

## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should obey the diagram plotted as below.



Note (1) The supply voltage of the external system for the module input should follow the definition of  $V_{CC}$ .

Note (2) Apply the LED voltage within the LCD operation range. When the backlight is turned on before the LCD operation or the LCD turns off before the backlight has been turned off, the display may momentarily become abnormal screen.

Note (3) In the case of  $V_{CC}$  is in off level, please maintain the level of input signals on the low or high impedance. If  $T2 < 0$ , that maybe cause electrical overstress failure.

Note (4)  $T4$  should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.



## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V <sub>CC</sub>	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I <sub>L</sub>	80±4.8	mA

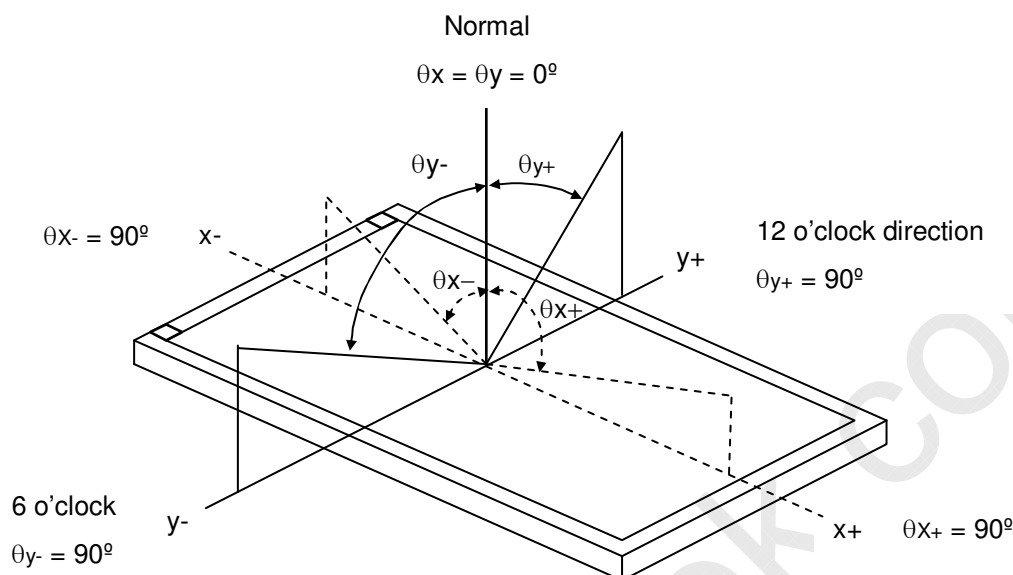
### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	2000	3000		-	(2)	
Response Time		Gray to Gray			8.5	14	ms	(3)	
Center Luminance of White		L <sub>C</sub>		320	400			(4)	
White Variation		δW				1.3	-	(7)	
Cross Talk		CT				4	%	(5)	
Color Chromaticity	Red	R <sub>x</sub>		Typ. -0.03	0.633	Typ. +0.03	-	(6)	
		R <sub>y</sub>			0.334		-		
	Green	G <sub>x</sub>			0.301		-		
		G <sub>y</sub>			0.630		-		
	Blue	B <sub>x</sub>			0.153		-		
		B <sub>y</sub>			0.057		-		
	White	W <sub>x</sub>			0.280		Target		
		W <sub>y</sub>			0.290				
	Color Gamut				CG			72	
Viewing Angle	Horizontal	θ <sub>x+</sub>	CR≥20	80	88		Deg.	(1)	
		θ <sub>x-</sub>		80	88				
	Vertical	θ <sub>y+</sub>		80	88				
		θ <sub>y-</sub>		80	88				

Note (1) Definition of Viewing Angle ( $\theta_x$ ,  $\theta_y$ ):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

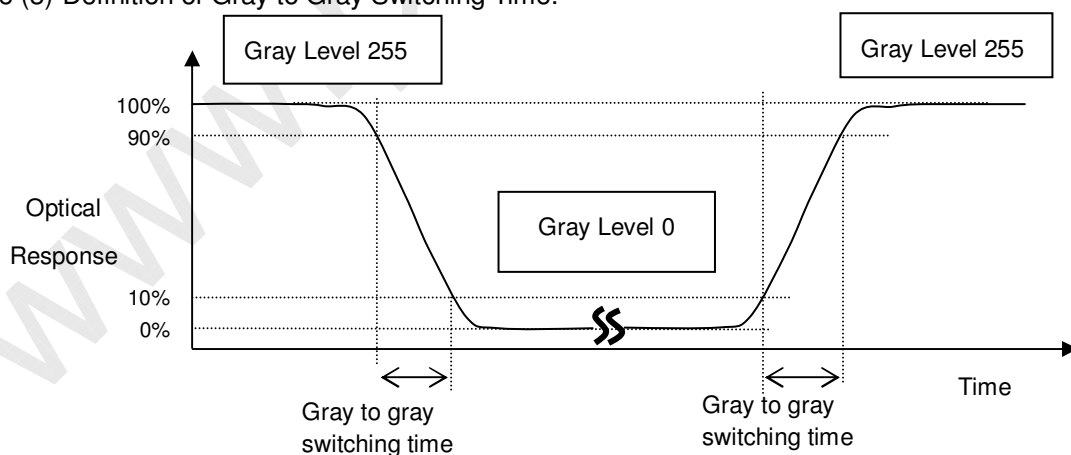
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X in the figure of Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of luminance 0%, 20%, 40%, 60%, 80%, and 100%.

Gray-to-Gray average time means the average switching time of luminance 0%, 20%, 40%, 60%, 80%, and 100% to each other.

Note (4) Definition of Luminance of White ( $L_C$ ):

Measure the luminance of gray level 255 at center point.

$L_C = L(5)$ , where  $L(x)$  is corresponding to the luminance of the point X in the figure of Note (7).

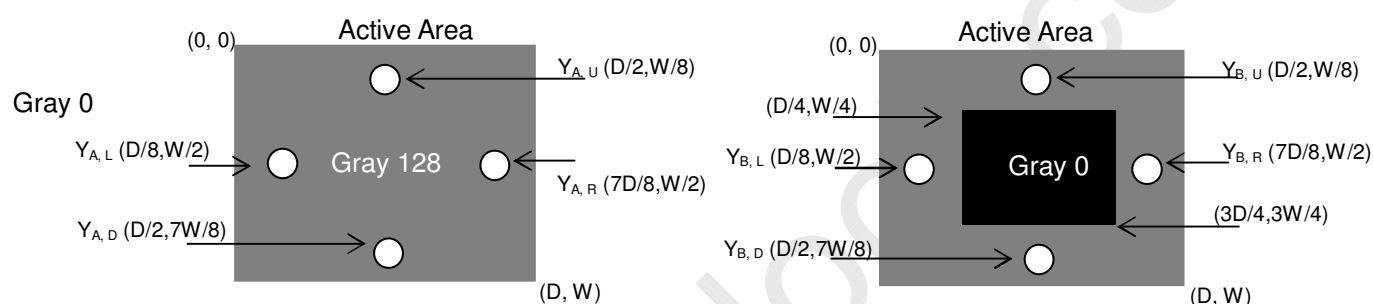
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

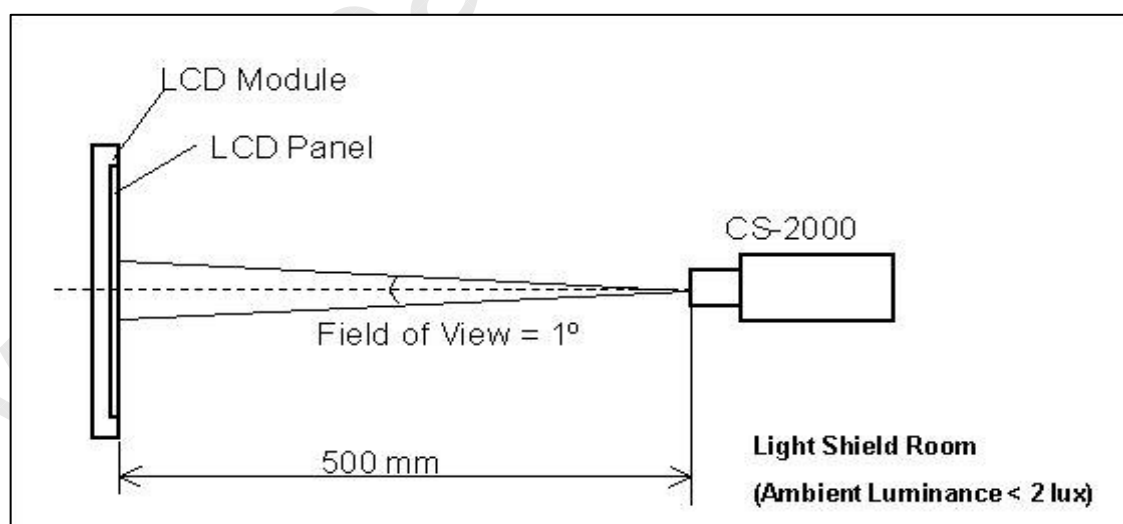
$Y_A$  = Luminance of measured location without gray level 0 pattern ( $\text{cd/m}^2$ )

$Y_B$  = Luminance of measured location with gray level 0 pattern ( $\text{cd/m}^2$ )



Note (6) Measurement Setup:

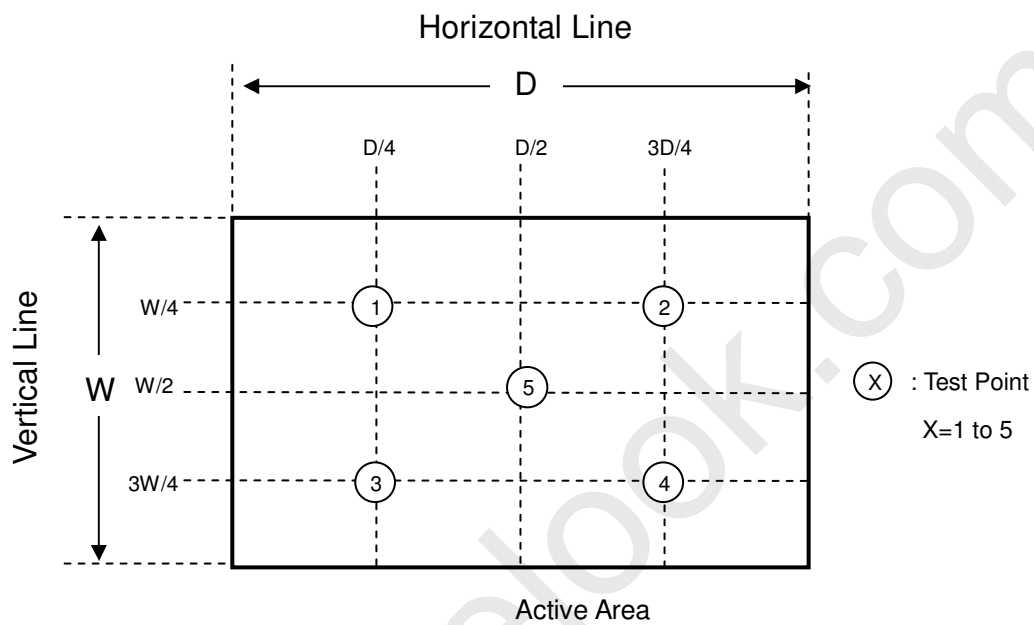
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation ( $\delta W$ ):

To measure the luminance of gray level 255 at 5 points

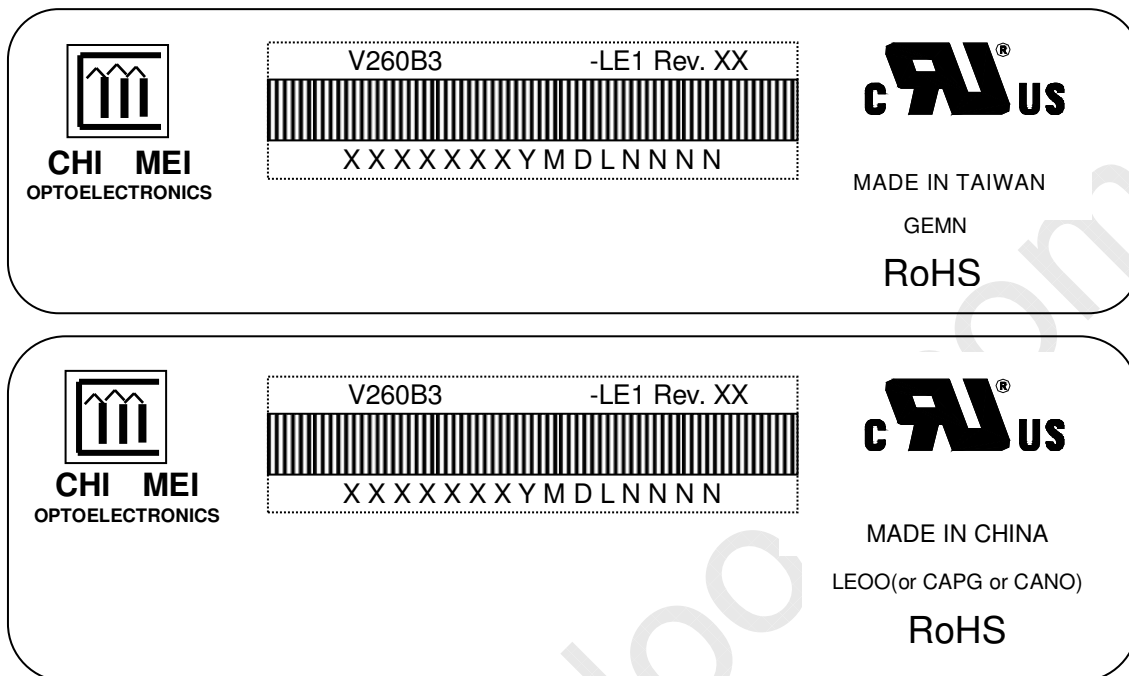
$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



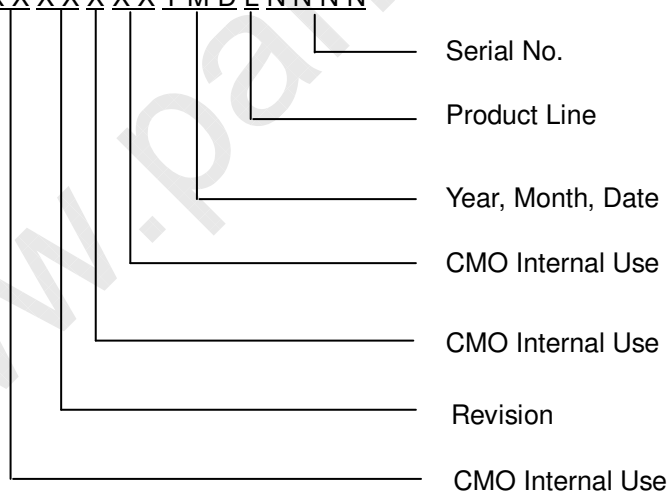
## 8. DEFINITION OF LABELS

### 8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V260B3-LE1  
 (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.  
 (c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019  
 Month: 1~9, A~C, for Jan. ~ Dec.  
 Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I, O, and U.  
 (b) Revision Code: Cover all the change  
 (c) Serial No.: Manufacturing sequence of product  
 (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

## 9. PACKAGING

### 9.1 PACKING SPECIFICATIONS

- (1) 11 LCD TV modules / 1 Box
- (2) Box dimensions : 698(L)x436(W)x452(H)mm
- (3) Weight : approximately 31.7 Kg (11 modules per box)

### 9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

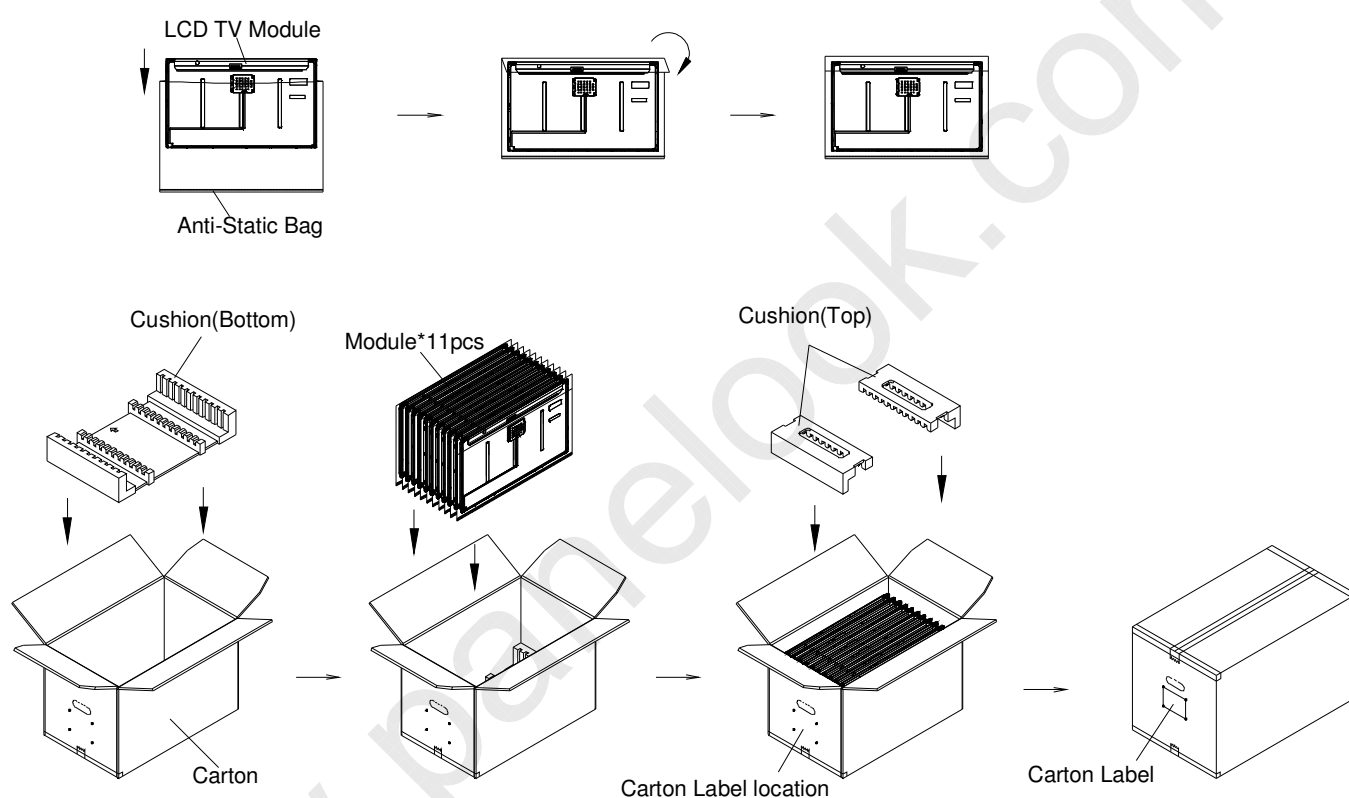


Figure 9-1 packing method

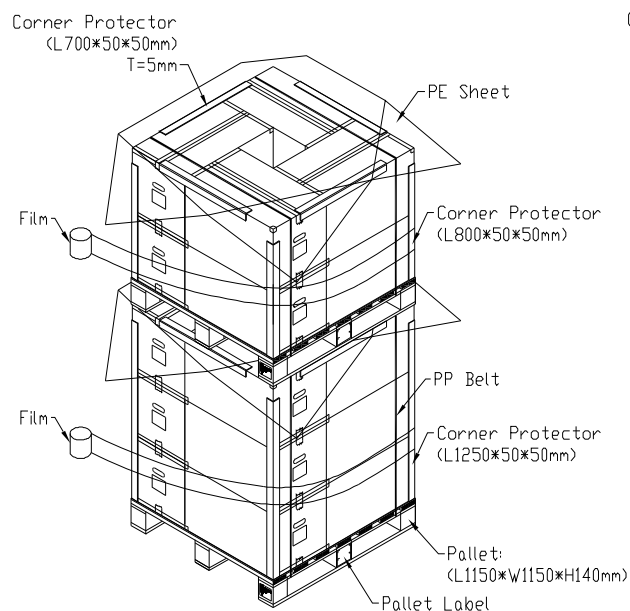
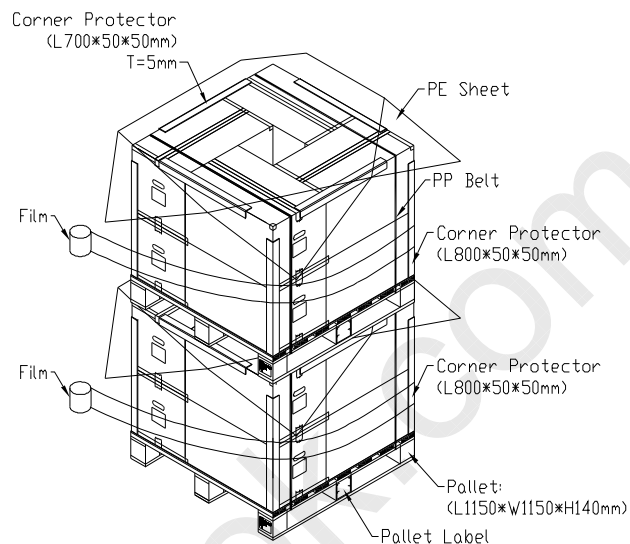
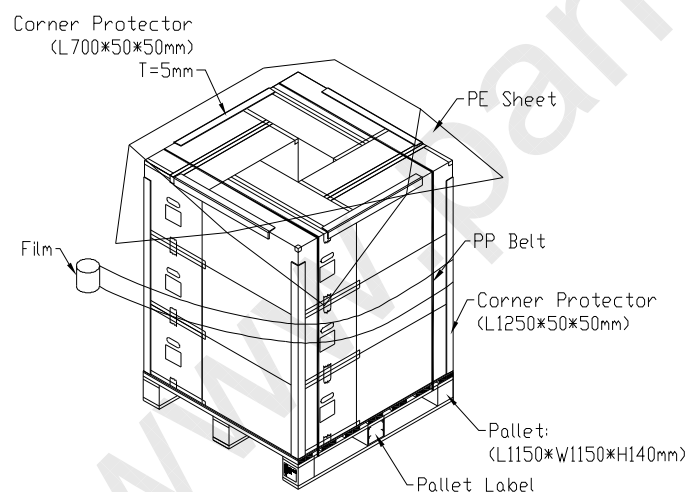
**Sea / Land Transportation  
(40ft HQ Container)****Sea / Land Transportation  
(40ft Container)****Air Transportation**

Figure 9-2 Packing method



## 10. PRECAUTIONS

### 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter or converter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

### 10.3 STORAGE PRECAUTIONS

When storing modules as spares for a long time, the following precaution is necessary.

- (1) Do not leave the module in high temperature, and high humidity for a long time.  
It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (2) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.





## 11. REGULATORY STANDARDS

### 11.1 SAFETY

The LCD module should be certified with safety regulations as follows:

Requirement	Standard	Remark
UL	UL60950-1:2006 or Ed.2:2007	
	UL60065 Ed.7:2007	
cUL/CSA	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07	
	CAN/CSA C22.2 No.60065-03:2006 + A1:2006	
CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009	
	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006 + A11:2008	

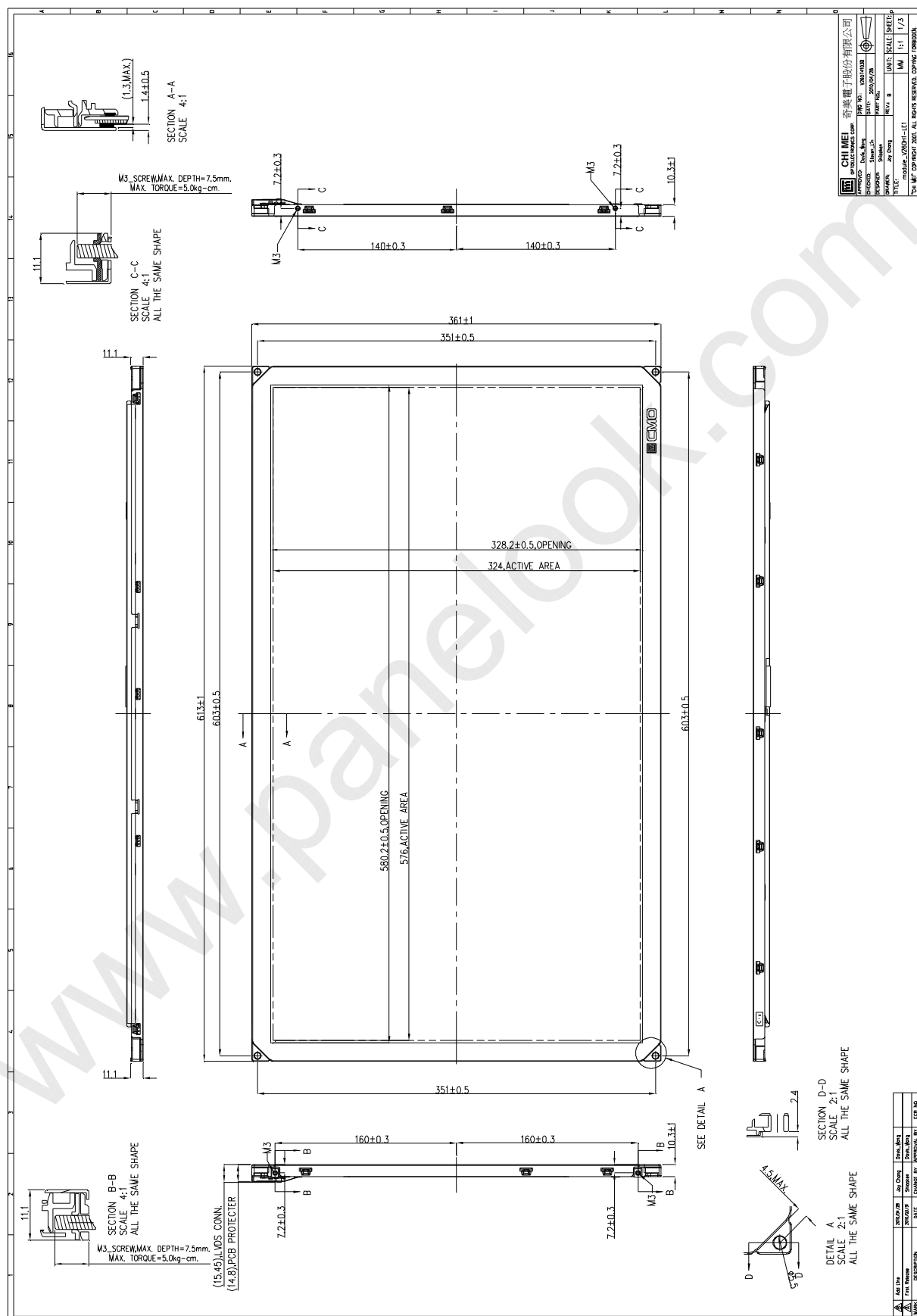
Issued Date: May. 17, 2010

Model No.: V260B3-LE1

**Approval**

**CHIMEI INNOVATION**

## 12. MECHANICAL CHARACTERISTIC





# CHIMEI INNOLUX

Issued Date: May. 17, 2010

Model No.: V260B3-LE1

**Approval**
